

AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Currently Amended) A semiconductor testing apparatus for testing semiconductor devices, configured to feed back data of returned samples which have been shipped as good samples, but returned from a user to a ~~manufacture~~ manufacturer as faulty samples so as to improve testing performance, the semiconductor testing apparatus comprising:

an IDDQ measuring circuit configured to measure current data of good samples and the samples ~~returned~~ returned by the user, by supplying test vector data to the good and returned samples;

a determination circuit configured to determine a range of pass/fail decision criteria and effective address pairs for testing target semiconductor devices based upon the measured current data,

wherein the IDDQ measuring circuit tests the target semiconductor devices by applying the test vector data for the effective address pairs.

2. (Previously Presented) The apparatus of claim 1 wherein the determination circuit comprises:

a changing rate calculation circuit configured to select a plurality of address pairs from the test vector data, to supply the address pairs to the good samples and the returned samples, to measure current-values of the good

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com